REMARKS

Applicants note with appreciation the finding that claims 3-4, 8-9 and 15-16 would be allowed if rewritten in independent form including all the limitations of the base claim and any intervening claims. (It is noted that at page 4 of the action, claims 14-16 are referenced rather than claims 15-16 as at page 1 of the office action.) Those claims have not been rewritten because it is submitted that the base claims should themselves be allowed.

Claims 1, 5-6 and 10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Aoki (U.S. Patent 6,087,864), and claims 2, 8, 13-14 and 17-18 were rejected under 35 U.S.C. 103 (a) as being unpatentable over Aoki. Those rejections are respectfully traversed and reconsideration is requested.

The present claims relate to a multiplier such as shown in the embodiment of Fig. 14. At page 12 of the specification, the embodiment of Fig. 14 is compared to the prior art of Fig. 16. In Fig. 16, an input signal aclk is applied to a phase comparator 194 and an output signal bclk is obtained from a voltage controlled oscillator 192. The output signal is divided down to produce a second input to the comparator dclk. As discussed at page 12, by dividing the output of the VCO, a clock dclk of the same frequency of the input signal aclk is obtained. These two clocks of the same frequency are then compared. Since the input clock is phase locked not to the high frequency output clock bclk, but rather to the output of the divider dclk, even when the loop is locked, the edges of aclk and bclk are not aligned.

By contrast, with the claimed invention, the phase comparator compares the phase of an edge of an input signal with the phase of an edge of the higher rate output signal. Thus, once the loop has aquired lock, the compared rising edges of aclk and bclk are exactly aligned, within the phase offset of the phase comparator. In the embodiment of Fig. 14, phase comparison of the edges of signals of different frequencies is enabled by a windowed phase comparator which receives a window signal, divided down from the output signal, which identifies the high frequency edges to be compared.

The Aoki reference suffers a problem similar to that of the prior art of Figure 16. In the cited Figure 1 of Aoki, as well as in the several embodiments disclosed in Aoki, a number of signals D0-Dz having the same frequency as the input signal ref are obtained. In the case of Fig. 1, those signals are obtained from a ring counter 30. In the various embodiments of Aoki, those signals are obtained from a delay chain 1. In each case, select ones of the signals D1-Dz, and perhaps the input signal, are applied to an exclusive NOR circuit to obtain the multiplied output 6. That the signal D0 is of the same frequency as input signal ref can be seen, for example, in Fig. 12.

Thus, it can be seen that in Aoki, as in the prior art Fig. 16 of the present application, it is not the higher rate output signal which is applied back to the phase comparator, but rather a signal D0 which is of the same rate as the input signal. Because there is no direct comparison of the higher frequency output signal with the input signal, exact alignment of those signals, within the phase offset of the phase comparator, cannot be obtained.

In finding anticipation by Aoki, the Examiner has stated that "the frequency generating circuit 30 of Fig. 1 of Aoki generates an output signal at a rate that is a multiple of input frequency" and that " a phase comparator (2)...compares the phase of an edge of the input signal (1) with the phase of an edge of the output signals (output from generator 30)." However, that interpretation is contrary to the literal wording of the claims. In particular, claim 1 recites "an output signal at a rate that is a multiple of input frequency." The ring counter 30 does not itself output a signal at a rate that is a multiple of the input frequency, though the ring counter 30 in combination with the exclusive NOR circuit 5 does output such a signal 6. However, the claim further recites that the phase comparator compares "the phase of an edge of the output signal." The second reference to "the output signal" is to the same signal recited in the first paragraph, that is, the output signal which has a rate that is a multiple of the input frequency. In Aoki, the signal applied to the phase comparator from the ring counter 30 is not the output signal 6 and is not at a rate that is a multiple of the input frequency. It is respectfully submitted that, to anticipate the independent claims, the same output signal having a rate that is a multiple of the

input frequency must also be applied to the phase comparator, and that is not the case in Aoki. Accordingly, the rejection is respectfully traversed and reconsideration is requested.

With respect to claims 2 and 7, the Examiner has stated that "it would be obvious to apply a window signal to the phase comparator for the advantage of controlling the timing of the operations of the phase comparator." However, Aoki teaches away from the claimed invention in that Aoki compares two signals of the same frequency. The window signal of the claimed invention distinguishes which edge of the high frequency output signal is to be compared against an edge of the low frequency input signal. When comparing two signals of the same frequency, there is no need to distinguish a particular edge. Aoki failed to recognize both the advantage of directly comparing the output signal with the input signal and the ability to perform such a comparison by using a window signal to select one edge of many in a high frequency signal to be compared with an edge of the low frequency signal.

For the same reasons that claims 15 and 16 are allowable, parallel method claims 11 and 12 should be allowable.

With respect to claims 13, 14, 17 and 18 it is respectfully submitted that there is no suggestion in the prior art of performing the claimed function in combinational logic (claims 13 and 17) or, more specifically, to use such combinational logic to provide current source and drain to an output as up and down current pulses (claims 14 and 18).

CONCLUSION

In view of the above remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned at (978) 341-0036.

Respectfully submitted,

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